Optimal Structure for High-Performance and Low-Contact-Resistance Organic Field-Effect Transistors Using Contact-Doped Coplanar and Pseudo-Staggered Device Architectures

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A low contact resistance achieved on top-gated organic field-effect transistors by using coplanar and pseudo-staggered device architectures, as well as the introduction of a dopant layer, is reported. The top-gated structure effectively minimizes the access resistance from the contact to the channel region and the charge-injection barrier is suppressed by doping of iron(III)trichloride at the metal/organic semiconductor interface. Compared with conventional bottom-gated staggered devices, a remarkably low contact resistance of 0.1–0.2 kΩ cm is extracted from the top-gated devices by the modified transfer line method. The top-gated devices using thienoacene compound as a semiconductor exhibit a high average field-effect mobility of 5.5–5.7 $cm^2 V^{-1} s^{-1}$ and an acceptable subthreshold swing of 0.23–0.24 V dec^{-1} without degradation in the on/off ratio of ≈10^9. Based on these experimental achievements, an optimal device structure for a high-performance organic transistor is proposed.

1. Introduction

Since the demonstration of the first organic field-effect transistor (OFET) in 1986, there has been much excitement for its potential application in low-cost and large-area consumer devices.[1,2] The reason is that organic materials can be deposited onto various kinds of substrate at low temperature, thus making a way for plastic electronics to be a key player in the electronics industry.[3] Moreover, the fabrication processes of OFETs are less technologically demanding than conventional crystalline silicon-based transistors.[2] Subsequently, much progress has been made over the last decade and the performance of the best organic materials has rivaled that of amorphous-silicon field-effect transistors, which have been traditionally used as switching elements in active matrix displays.[3]

Despite the numerous advantages of OFETs, one of the serious issues facing OFETs is their relatively high contact resistance (R_c), which limits the electrical performance and scaling potential of OFET devices.[4–9] The large R_c lowers the field-effect-mobility (μ_{FET}) value and results in a poorer subthreshold swing (SS), in addition to a shift in the device threshold voltage (V_T).[8] Furthermore, in short-channel devices, the contribution of the R_c to the total resistance (R_{total}) of the device becomes more significant as it contributes a larger fraction of R_{total}.[3] The exact origin of the contact resistance is still an on-going study, but it has been generally attributed to a work function mismatch between the Fermi level of the electrode and the highest occupied molecular orbital (HOMO) of the *p*-type organic semiconductor, as well as the charge traps in the access region between the contact and the channel.[6–8,10] One common approach to suppress the R_c is through modification of the source/drain-contacts, for instance by the insertion of an injection-assist layer such as molybdenum oxide,[8,11] or the application of a self-assembled monolayer[12,13] and, more recently, an ultrathin insulating oxide such as aluminum oxide.[14] Significantly, a small R_c has been reported in the literature in OFETs based on pentacene and C_{60}, where R_c values as low as 0.08 and 0.58 kΩ cm have been obtained respectively.[15,16] These studies were based on bottom-gate and bottom-contact coplanar devices, in which the contacts were treated with hexamethyldisilazane vapor[16] and UV-ozone[15] respectively in order to increase the work function of the contact. The large crystal grain sizes near the contact may also contribute to the reduction of the contact resistance.

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In this work, we propose an optimal device structure in which the R_c can be minimized, by choosing/designing an appropriate device architecture. In previous work, we reported the contribution of the access resistance (R_{access}) to R_c, which is caused by charge-transport processes in the bulk of the semiconductor from the contact to the channel, in which charge carriers must traverse from the source contact to the accumulation layer (the channel) at the semiconductor-insulator interface and then back to the drain contact to be extracted.[3,6–8] Thus, the metal/organic interface resistance caused by the charge-injection barrier (R_{int}) and R_{access} can be two significant factors which affect the R_c. This is illustrated schematically by the bottom-gate top-contact (BGTC)-device staggered architecture shown in **Figure 1**a. Therefore, based on this understanding, R_c can be minimized by suppressing the contribution of both R_{int} and R_{access}. In this report, we show that R_{int} and R_{access} can be suppressed by the introduction of a dopant layer at the contact and by using an appropriate device architecture, respectively. We introduce a strong-acceptor-type dopant into the contact interface to reduce R_{int}, and choose the top-gate structures to directly connect the doped region at the contact and charge accumulation region to reduce R_{access}. We demonstrate that by choosing an appropriate contact and semiconductor layer thickness, the R_{access} can be made significantly smaller, even in the staggered device architecture. The smaller R_c can lead to further enhancement of the OFET electrical performance. A thienoacene-based organic semiconductor was used in this study. Recently, a printed, high-quality single crystal of the organic semiconductor 2,7-dioctyl[1]-benzothieno[3,2-b][1]benzothiophene (C8-BTBT) was reported to have a high average μ_{FET} mobility of 16.4 $cm^2 V^{-1} s^{-1}$, which is on par with polycrystalline-silicon thin-film transistors, and is the highest performance obtained for rubrene single-crystal devices.[17] In this work, we show that by using appropriate device architectures, we can obtain a high average mobility and on/off ratio with minimized R_c in OFETs.

2. Results and Discussions

The schematics of the fabricated devices with top-gate bottom-contact (TGBC) and top-gate top-contact (TGTC) configurations are illustrated in Figure 1b and 1c. The OFETs were fabricated on a glass substrate. Apart from the Cytop (Asahi Glass Co.) gate dielectric, which was spin-coated, all of the deposition processes were carried out by thermal evaporation. The $FeCl_3$ doping layer was inserted into the electrode/semiconductor interface for both the TGBC and TGTC devices, which are referred to as TGBC-doped and TGTC-doped, respectively, depending on their device architecture. The TGTC device had a coplanar structure where the doped region at contact was in the vicinity of the channel. For TGBC devices, the same film thickness was used for the semiconductor and the bottom-contact electrodes, in which the doped region at the contact was very close to the channel region (a pseudo-staggered structure). We have used the term pseudo-staggered as a reminder that although in theory a TGBC device is a staggered architecture, the closeness of the channel to the doped region of the contact is similar to that of a coplanar device. As a reference, we fabricated the TGBC and TGTC structures without the $FeCl_3$ doping layer, which are referred to in the manuscript as TGBC-ref and TGTC-ref, respectively. For a comparison, we show the results of the bottom-gate top-contact (BGTC) devices with and without doping of $FeCl_3$ at the electrode interface, which are represented as BGTC-doped and BGTC-ref, respectively.[18] The transistor performance was characterized in the dark and under vacuum conditions (≈10^{-4} Pa).

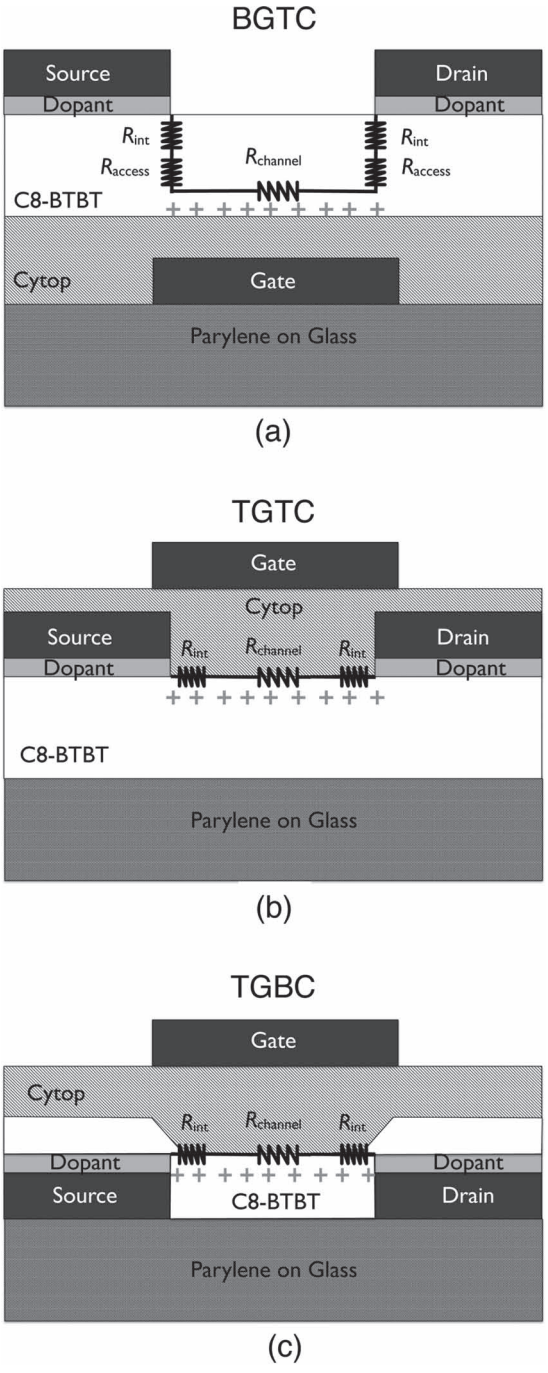

Figure 1. a–c) Schematic illustration of conventional BGTC staggered (a), TGTC coplanar (b), and TGBC pseudo-staggered (c) device architectures. In the case of (a), the contribution to R_{access} is significant, whereas in (b) and (c), the contribution of R_{access} is diminished, leading to a lower R_c.

The R_c was obtained from the transfer curves of the OFETs measured in the linear region at a drain-source voltage (V_{DS}) of −1.0 V. The modified transfer line method (M-TLM) was employed to determine the R_c from the various channel lengths. The M-TLM method allows a more-accurate evaluation of the R_c through simple modification of the conventional TLM based on Equation 1 below:[19]

$$\frac{R_{total}W}{L} = \frac{1}{\mu C_i (V_{GS} - V_T)} + \frac{R_c W}{L} \quad (1)$$

where R_{total} is the total resistance of the OFETs, L and W are the channel length and width, μ is the mobility and C_i is the capacitance of the gate dielectric. V_{GS} and V_T are the gate-source voltage and threshold voltage, respectively. As shown in Equation 1, R_c can be obtained from the slope of a linear regression fit to $R_{total}W/L$ as a function of $1/L$. The main advantage of this methodology is that the R_c of the devices directly controls the linear regression of the fitted M-TLM plots, as opposed to the conventional TLM. This method is described in detail in the work of Xu et al.[19] We measured the L of the fabricated OFETs accurately using a standard microscope ruler to determine the R_c accurately by the M-TLM. **Figure 2**a–e show M-TLM plots of BGTC-ref, BGTC-doped, TGBC-ref, TGBC-doped, and TGTC-doped, respectively. The extracted values of R_c from the slopes of the M-TLM plots are 200, 8.5, 1.8, 0.1, and 0.2 kΩ cm, at V_{GS} = −40 V for the BGTC-ref, BGTC-doped, TGBC-ref, TGBC-doped, and TGTC-doped, respectively (**Table 1**). The obtained R_c values for the OFETs are shown in Figure 2f as a function of V_{GS}. As we have previously reported, the R_c of the BGTC devices can be significantly reduced from 200 to 8.5 kΩ cm by the doping of $FeCl_3$ into the electrode interface.[18] On the other hand, the M-TLM results indicate that further lowering of R_c is possible by use of a top-gated device structure. In particular, exceptionally low R_c values of 0.1 and 0.2 kΩ cm were obtained for TGBC-doped and TGTC-doped devices, respectively.

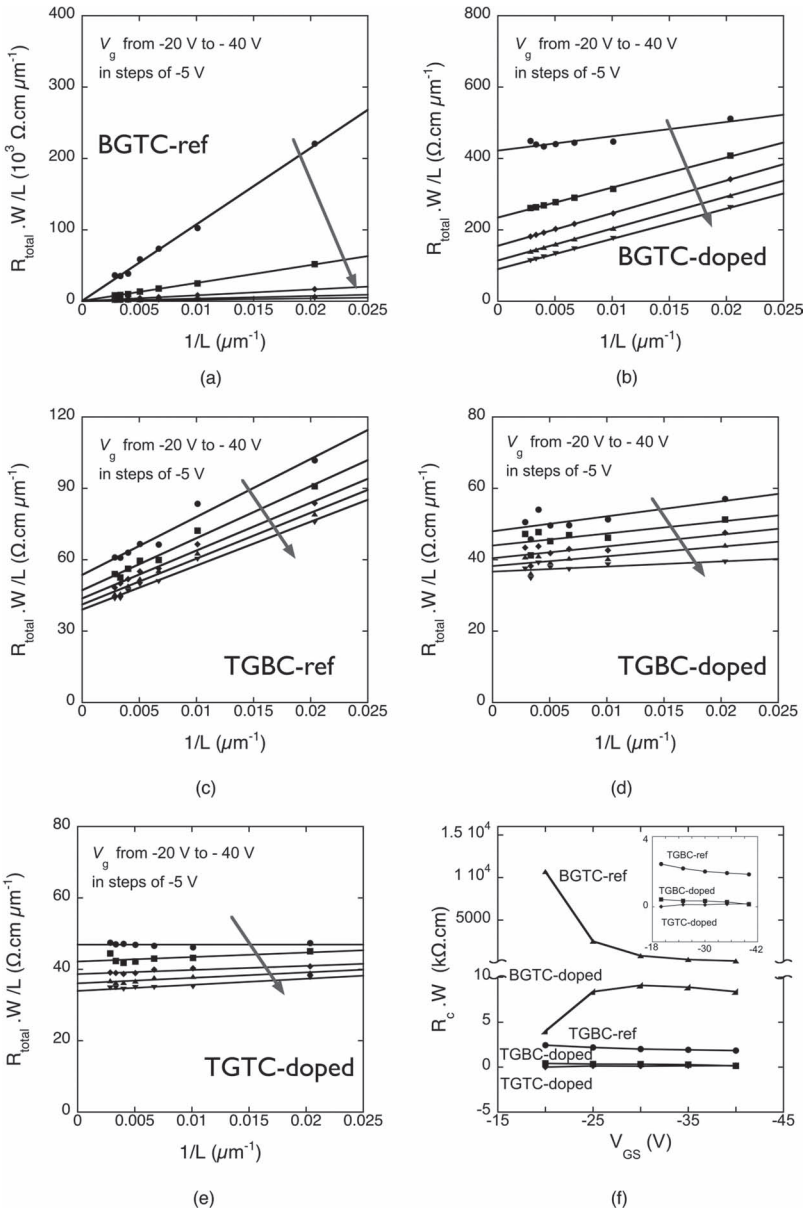

Figure 2. a–e) M-TLM plots for BGTC-ref(a), BGTC-doped (b),TGBC-ref(c), TGBC-doped (d), and TGTC-doped (e) TGTC-doped devices at various gate voltages. The slope of the linear regression fit denotes the R_c. f) Summary of thecontact resistance changes of the various devices as a function of the gate voltage. The inset in (f) denotes the contact resistance variance with gate voltage for TGBC-ref, TGBC-doped, and TGTC-doped devices for clarity.

Table 1. Summary of the electrical characteristics of the fabricated devices.

Samples	Device Architecture	Dielectric	Dielectric constant, κ	Threshold voltage, V_T [V]	Field-effect mobility, μ_{FET} [cm^{-2} V^{-1} s^{-1}]	Subthreshold swing, SS [V dec^{-1}]	Contact resistance, R_C [kΩ cm]
BGTC-ref	Staggered	Parylene	3.1	−25[a)]	3.4[a)]	2.4[a)]	200[a)]
BGTC-doped	Staggered	Parylene	3.1	−10[a)]	7.0[a)]	0.21[a)]	8.5[a)]
TGBC-ref	Pseudo-staggered	Cytop	2.1	−2.2	2.2	0.70	1.8
TGBC-doped	Pseudo-staggered	Cytop	2.1	−0.81	5.5	0.24	0.1
TGTC-doped	Coplanar	Cytop	2.1	1.1	5.7	0.23	0.2

[a)]Based on previous work.[18]

The origin of the significant reduction in R_c by use of the top-gated structure is discussed below.

A large reduction in R_c for the TGBC-doped and TGTC-doped devices was achieved by suppression of two factors, R_{int} and R_{access}, by employing contact doping and a coplanar or pseudo-staggered device architecture. The suppression of R_{int} by the introduction of the $FeCl_3$ dopant into the contact interface can be explained through the reduction of the depletion-region (Schottky like barrier) width and, consequently, the occurrence of field-emission tunneling through the thinner depletion layer. In our experiments, a photoelectron yield spectroscopy (PYS) measurement revealed that the ionized potential of C8-BTBT was 5.4 eV, which is much larger than the work function (W_F) of the vacuum-deposited Au electrode of 4.6 eV, measured in a similar manner using PYS.[18] Thus, the depletion layer was formed at the metal/semiconductor interface due to charge transfer between the electrode and semiconductor. The addition of a dopant layer at the contact interface may increase the charge density in the depletion layer, which would in turn reduce the width of the depletion region, thus promoting a more-efficient charge injection through the thinner depletion layer. This occurrence will inevitably lead to the reduction of R_c as the contribution of R_{int} is suppressed.

The other factor that significantly reduces R_c is the suppression of R_{access} by employing a coplanar or pseudo-staggered device structure. The strategy in employing a coplanar device architecture in order to obtain better device performance has also been used by other research groups.[20] As mentioned above, in the conventional staggered structure of the BGTC devices, a significantly high R_c value of 200 kΩ cm was obtained at V_{GS} = −40 V by M-TLM analysis of the BGTC-ref sample. The R_c value was reduced to 8.5 kΩ cm by the introduction of $FeCl_3$ into the contact. However, a further reduction in R_c could be achieved by employing an appropriate device architecture (Table 1). The low R_c values of 0.1 and 0.2 kΩ cm for the TGBC-doped and TGTC-doped devices, respectively, were due to the diminishment of the access region by the coplanar and pseudo-staggered device structures. The coplanar structure is widely used as a bottom-gate bottom-contact (BGBC) structure in OFETs, and a relatively large R_c is often reported for this device structure because the grain size of the organic semiconductor tends to be small near the bottom-contact electrode.[3,21] The R_c of the BGBC devices is considered to be dominated by this low-conductive region near the contact, which is often modeled as a depletion region.[9,13,22,23] In the work of Xu et al. and Singh et al., they adopted a planar device architecture in order to achieve a continuous organic semiconductor grain across the contacts, thereby reducing the depletion region.[20] On the other hand, a very low R_c is sometimes reported for BGBC coplanar devices if large grains can be formed at the contact edge.[3,15,24] We utilized the TGTC architecture as a coplanar structure and introduced the dopant at the electrode/semiconductor interface in the coplanar devices. We also used the TGBC devices as a pseudo-staggered structure, where the same film thickness was employed for the bottom source/drain electrodes and the organic semiconductor layer. The dopant layer was introduced on top of the bottom electrodes, as the doped contact region was located in the vicinity of the channel region (Figure 1c). As a result, in these top-gated structures, the channel region was directly connected to the $FeCl_3$ doped region at contact (Figure 1b,c) and the access region between the contact and the channel was diminished.

In Figure 2f and Table 1, even the TGBC-ref sample shows a much lower R_c than the BGTC devices. This result implies that the contribution of R_{access} to R_c is crucial, and the top-gated structure effectively reduces the R_{access}. Another interesting observation seen in Figure 2f is the difference in the V_{GS} dependence of R_c for each device. It is widely known that the R_c of OFETs exhibits a V_{GS} dependence. The possible origin of the V_{GS} dependence of R_c in OFETs could be the modulation of the depletion layer thickness by V_{GS}[4,25] or could be as a result of charge transport in the trap-rich access region.[23] Compared with the large V_{GS} dependence of R_c in the BGTC-ref device (Figure 2f), the top-gated devices showed a much smaller V_{GS} dependence of R_c. On the other hand, in the inset of Figure 2f, the R_c of the TGBC-ref device showed a slight but obvious R_c dependence, while almost no V_{GS} dependence of R_c was observed for the TGTC-doped device. The disappearance of the V_{GS} dependence of R_c in the TGTC-doped device may indicate the complete suppression/removal of the depletion layer at the contact and the access region by the contact doping and the top-gated device structure.

Figure 3a,b show the typical transfer characteristics of TGBC-doped and TGTC-doped OFETs with a channel length (L) of 100 μm. The addition of the $FeCl_3$ dopant layer at the source/drain contact caused a pronounced improvement to the drain current in both the TGBC-doped and TGTC-doped devices. Also evident from the transfer curve (Figure 3a,b) is the disappearance of the hysteresis found in the TGBC-ref device (Figure S1a, Supporting Information) upon the introduction of the source/drain dopant layer. The presence of hysteresis is typically attributed to charge trapping at the shallow trap states in the organic semiconductor or trapping at the metal/organic semiconductor interface. The disappearance of the hysteresis clearly indicates the reduction of charge traps at the contact interface by the doping of $FeCl_3$. The average field-effect mobilities of over 20 fabricated devices were determined to be 2.2, 5.5 and 5.7 $cm^2\ V^{-1}\ s^{-1}$ for the TGBC-ref, TGBC-doped and TGTC-doped devices, respectively. The results are summarized in Table 1 alongside a comparison with the BGTC devices based on our previous report.[18] The V_T was generally low across all of the top-gate devices, with a slight improvement in both the TGBC-doped and TGTC-doped devices, with −2.2, −0.81, and 1.1 V for the TGBC-ref, TGBC-doped, and TGTC-doped devices, respectively. In addition, acceptable SS values of 0.70, 0.24, and 0.23 V dec^{-1} were obtained for the TGBC-ref, TGBC-doped, and TGTC-doped samples, respectively. In comparison with previous work on C8-BTBT devices by Endo and co-workers[26] and Minari and co-workers,[18] the SS presented in this work is smaller or comparable (for similarly doped devices). Other research groups working on other organic semiconductor materials have managed to obtain even-sharper SS values, lower than 0.1 V dec^{-1}, with some approaching the theoretical limit for an Ohmic charge injection from a metal to a semiconductor at room temperature.[27] However, it must be noted that the dielectric thickness used in this work was much thicker than the reported work with the sharper SS. In that sense, the SS reported in this work could potentially be

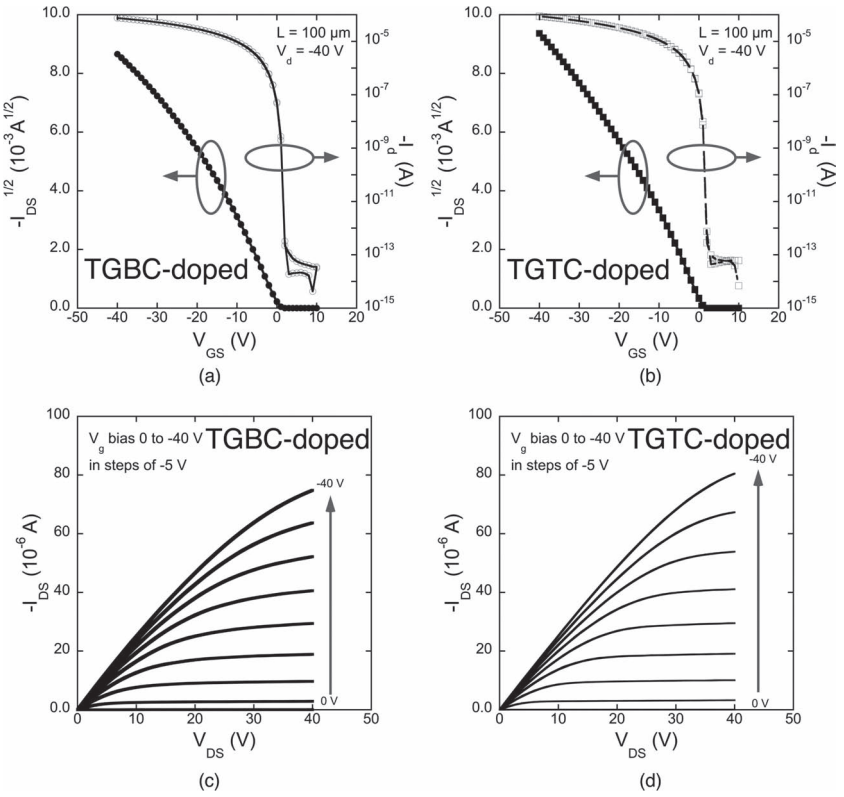

Figure 3. a,b) Transfer characteristics: square root of the drain current ($I_{DS}^{1/2}$) (left axis) and drain current (I_{DS}) (right axis) versus gate voltage (V_{GS}) at drain voltage (V_{DS}) = −40 V (saturation mode) of TGBC-doped (a) TGBC-doped and TGTC-doped (b) devices with a channel length of 100 μm. c,d) Output characteristics (I_{DS} versus V_{DS}) of TGBC-doped (c) TGBC-doped and TGTC-doped (d) TGTC-doped devices. Linear and proportional I_{DS}–V_{DS} behavior is clearly shown at low V_{DS} and a significant improvement of the output current in the doped devices is clearly exhibited.

improved by employing a much thinner gate dielectric layer. It has been reported that the SS is affected by charge traps at the metal/organic semiconductor interface, as well as by traps at the insulator/organic semiconductor interface. The lower SS obtained from the TGBC-doped and TGTC-doped devices was clearly due to the reduction in charge-trap states at the contact interface. Furthermore, a high on/off current-switching ratio ($I_{on/off}$) of ≈10^9 was attained using the fabricated top-gated devices. In comparison with the bottom-gated device obtained from our previous work, the top-gated devices showed a remarkably lower V_T, while maintaining similar values to both μ_{FET} and SS.[18] A low V_T, a good subthreshold swing, and a low off current are important considerations for low-power device applications.

The output characteristics of the devices (Figure 3c,d) showed clear current saturation at $V_{DS} > (V_{GS}-V_T)$ and very proportional linear behavior in the low V_{DS} region, suggesting a potentially low R_c and an Ohmic-like contact. It was shown that for a channel length of 100 μm, the doped devices (Figure 3c,d) showed better electrical characteristics as compared with the undoped device (Figure S1b). The channel length of 100 μm used in this study is much longer than that normally used in amorphous silicon thin-film transistors (a-Si TFTs), 1–2 μm. On the other hand, the μ_{FET} of our devices was about one order of magnitude higher than that of conventional a-Si thin-film transistors (TFTs), which exhibit a high potential for use in practical applications. The very low values of R_C achieved in this work also imply that we can further reduce the L of the TGTC-doped and TGBC-doped devices.

In order to gain further insight into the improvements observed in the device electrical performance, a temperature-dependent measurement on the TGTC-doped device was performed. As seen in **Figure 4**a, the measured drain current increased with increasing temperature. The inset in Figure 4b shows a plot of extracted linear mobility (μ_{lin}) (at V_{DS} = −1 V) against temperature. The linear fit and positive $d\mu_{lin}/dT$ suggests a thermally activated hopping in localized states, consistent with our expectations for polycrystalline C8-BTBT, which should exhibit a similar charge transport mechanism to polycrystalline pentacene.[9,28] Subsequently, μ_{lin} was plotted against $1/T$ in order to ascertain the activation energy (E_a), by the following equation:[29]

$$\mu_{lin} = \mu_0 \exp\left(\frac{-E_a}{k_B T}\right) \quad (2)$$

where μ_0 is a prefactor, k_B is the Boltzmann constant, and T is the temperature in Kelvin. Based on Equation 2, the E_a could be determined from the slope of the plot of μ_{lin} versus $1/T$ as being 9.2 meV. The E_a obtained in this work for C8-BTBT is

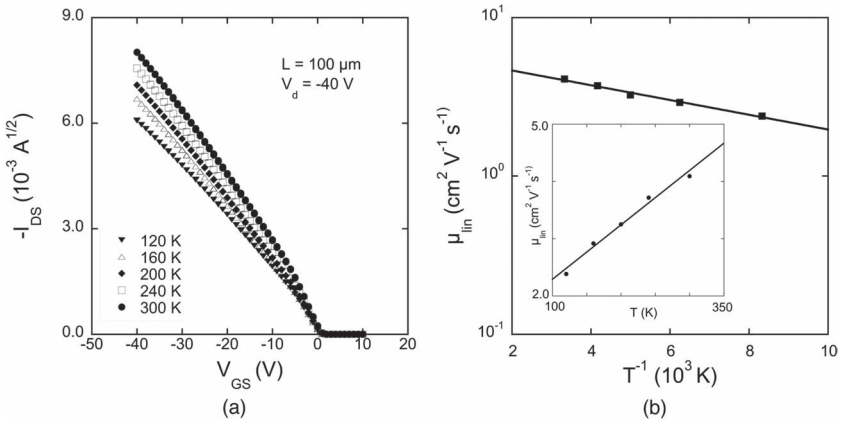

Figure 4. a) Transfer curves of the TCTG-doped device with L = 100 μm in the linear region (V_{DS} = −1 V) at various temperatures. b) Linear region mobility as a function of $1/T$. The activation energy is extracted from the slope of the linear regression fit of μ_{lin} versus $1/T$. Inset: Linear regression fit of $d\mu_{lin}/dT$, indicating a thermally activated hopping charge-conduction mechanism.

much lower than that of pentacene-based OFETs, which has been reported to be in the range of 38–128 meV.[7,30] As such, it is also reasonable to suggest that, possibly, the charge-transport mechanism is not dominated by thermally activated hopping alone, but rather through a combination of thermal hopping and band-like transport. This could explain the large drain current obtained in the TGTC-doped devices and the subsequent high mobility, which is comparable with that of single-crystal C8-BTBT OFETs.[31]

3. Conclusions

In summary, we have shown that an exceptionally low R_c can be obtained in an OFET device through the reduction of R_{access} and R_{int}, which is achieved by using an optimal device structure and the introduction of a dopant layer at the contact. R_c values of 0.1 and 0.2 kΩ cm were obtained for the TGBC-doped and TGTC-doped devices, respectively. These top-gated devices showed average μ_{FET} and SS values of 5.5–5.7 $cm^2\ V^{-1}\ s^{-1}$ and 0.23–0.24 V dec^{-1}, respectively, with a near-zero V_T and a high $I_{on/off}$ of $\approx 10^9$. This remarkable performance is a result of the nearly Ohmic contact, which is evidenced by the proportional output curve in the linear region. This result may facilitate further down-scaling of OFET devices for their integration into practical applications.

4. Experimental Section

The OFET devices were fabricated on glass substrates. The substrate was first cleaned using a standard cleaning process of ultrasonification through acetone and isopropyl alcohol solution for 5 min, followed by UV-plasma cleaning. A thin layer (290 nm) of parylene (Dix-C) film was formed on the substrate through chemical vapor deposition to ensure a good-quality C8-BTBT film. For the TGBC-ref device, the source/drain electrodes were formed by vacuum evaporation of Au through a physical shadow mask to a thickness of 40 nm. As for the TGBC-doped-device, a thin layer of a 0.3 nm $FeCl_3$ dopant layer was deposited by vacuum evaporation through the physical shadow mask right after the Au source/drain formation. This was followed by vacuum evaporation of C8-BTBT organic semiconductor material trough the physical shadow mask to a thickness of 40 nm. Next, the gate insulator, Cytop (Asahi Glass), was spin-coated onto the substrate at a speed of 500 rpm for 5 s, followed by 4000 rpm for 60 s. This formed a uniform Cytop film, 535 nm in thickness. The Au top-gate was then formed through vacuum evaporation on the Cytop through a physical shadow mask to a thickness of 40 nm. In the case of the fabrication of the TGTC-doped device, the C8-BTBT organic semiconductor was first evaporated on Dix-C film through a physical shadow mask to a thickness of 40 nm. After that, a thin, 0.3 nm $FeCl_3$ dopant layer was deposited by vacuum evaporation through the physical shadow mask, followed by Au metal source/drain vacuum evaporation for 40 nm. Next, the gate insulator C_{YTOP} (Asahi Glass) was spin-coated onto the substrate at a speed of 500 rpm for 5 s, followed by 4000 rpm for 60 s (535 nm thickness). Finally, the Au top-gate was then formed through vacuum evaporation on the Cytop through a physical shadow mask to a thickness of 40 nm. OFETs of various lengths of 50 to 350 μm and a width of 1000 μm were prepared in order to evaluate the R_c through M-TLM. Electrical measurements on the OFET devices were carried out in the dark and in a vacuum using a 4156C Agilent precision semiconductor analyzer. In the low-temperature electrical measurement, liquid nitrogen was used to cool down the substrate in the vacuum measurement chamber.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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